Course code: **20EC4210** **R20**

**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNNOLOGY :: PUTTUR**

Siddharth Nagar, Narayanavanam Road – 517583

**QUESTION BANK (DESCRIPTIVE)**

| | | | |
|---|---|---|---|
| **Subject With Code:** | Low Power VLSI Design (20EC4210) | **Course & Branch:** | M.TECH-VLSI DESIGN |
| **Regulation:** | R20 | **Year & Sem:** | I M.Tech & II SEM |

## UNIT –I

## LOW POWER DESIGN, AN OVER VIEW & MOS/BiCMOS PROCESSES

| | | | | |
|---|---|---|---|---|
| 1. | a) | What are the various limitations of Low-voltage, Low-power design? | [L2][CO2] | **[6M]** |
| | b) | Explain about Silicon-on-Insulator (SOI) technology. | [L2][CO1] | **[6M]** |
| 2. | a) | Explain low cost, medium speed digital CMOS process. | [L2][CO2] | **[6M]** |
| | b) | Draw the structure of P-well BiCMOS process and explain the same. | [L1][CO3] | **[6M]** |
| 3. | a) | Draw the structure of Twin-well BiCMOS process and explain the same. | [L1][CO3] | **[6M]** |
| | b) | Explain in detail about threshold voltage adjustment for CMOS devices | [L3][CO1] | **[6M]** |
| 4. | | With suitable diagram, Explain the following,<br>a) Phosphorous Drain Structure,<br>b) Double Diffused Drain,<br>c) Lightly Doped Drain. | [L1][CO2] | **[12M]** |
| 5. | | Describe different process considerations for Bipolar transistors. | [L2][CO1] | **[12M]** |
| 6. | a) | How the bipolar transistor takes important role in Isolation in BiCMOS? | [L1][CO3] | **[6M]** |
| | b) | How the MOS transistor takes important role in Isolation in BiCMOS? | [L3][CO2] | **[6M]** |
| 7. | a) | What are the considerations for process integration in BiCMOS process? | [L1][CO1] | **[6M]** |
| | b) | What are the considerations for typical analog/Digital BiCMOS process? | [L2][CO3] | **[6M]** |
| 8. | | Briefly describe LOCOS isolation technique in MOS transistors with neat sketch. | [L1][CO1] | **[12M]** |
| 9. | a) | Explain about punch through in short – channel MOSFETS. | [L2][CO3] | **[6M]** |
| | b) | Describe different process considerations for Bipolar transistors. | [L1][CO1] | **[6M]** |
| 10. | | Explain the following with neat diagrams,<br>a) Shallow trench Isolation,<br>b) Deep trench Isolation. | [L3][CO2] | **[12M]** |

Course code: **20EC4210** **R20**

## UNIT-II

## LOW-VOLTAGE/LOW POWER CMOS/ BiCMOS PROCESSES & DEVICE BEHAVIOR AND MODELING

| | | | | |
|---|---|---|---|---|
| 1. | a) | With the help of neat sketches explain about Poly silicon Emitter High-performance BICMOS structures and Explain about the process steps. | [L2][CO3] | **[6M]** |
| | b) | Explain the low capacitance Bipolar/BiCMOS processes with neat diagram. | [L1][CO1] | **[6M]** |
| 2. | a) | Explain the SOI CMOS/BiCMOS VLSIs processes. | [L3][CO2] | **[6M]** |
| | b) | Explain in detail about copper Electroplating/Copper-Fill. | [L1][CO1] | **[6M]** |
| 3. | | With neat diagram explain in detail about SOI BiCMOS structures with copper metallization. | [L1][CO3] | **[12M]** |
| 4. | a) | Describe the device structure and fabrication process for lateral BJT on SOI. | [L1][CO2] | **[6M]** |
| | b) | What are the electrical characteristics of lateral BJT on SOI? | [L2][CO1] | **[6M]** |
| 5. | | What are the future trends and directions in CMOS/BICMOS processes? Explain. | [L2][CO3] | **[12M]** |
| 6. | | Explain the following Advanced MOSFET models,<br>a) HSPICE level 50 Model,<br>b)EKV MOSFET Model. | [L3][CO1] | **[12M]** |
| 7. | a) | What are the limitations of the MOSFET characteristics? | [L2][CO1] | **[6M]** |
| | b) | Explain in detail about MOSFET device fabrication in Hybrid-Mode Environment. | [L1][CO1] | **[6M]** |
| 8. | a) | What are the future trends and directions in CMOS/BICMOS processes? Explain. | [L1][CO1] | **[6M]** |
| | b) | Briefly explain LEVEL4 MOSFET Spice model. | [L2][CO3] | **[6M]** |
| 9. | | Explain the following Bipolar spice models,<br>a) Ebers-Moll model,<br>b) Modified Gummel-Poon Model. | [L1][CO1] | **[6M]** |
| 10. | a) | Describe briefly about VBIC95 Bipolar spice model. | [L3][CO2] | **[6M]** |
| | b) | Explain the Noise model of HSPICE Level 50. | [L1][CO1] | **[6M]** |

Course code: **20EC4210** **R20**

## UNIT III

## CMOS AND Bi-CMOS LOGIC GATES & LOW- VOLTAGE LOW POWER LOGIC CIRCUITS

| | | | | |
|---|---|---|---|---|
| 1. | a) | Explain the following parameters in conventional CMOS logic gates,<br>a)Power dissipation in CMOS technology,<br>b)Complementary MOS Inverter. | [L1][CO1] | **[6M]** |
| | b) | Design basic NOR and NAND gate using conventional CMOS logic gates. | [L1][CO3] | **[6M]** |
| 2. | a) | Describe the basic driver configuration in conventional Bi CMOS logic gates. | [L2][CO3] | **[6M]** |
| | b) | Explain the following parameters in conventional Bi CMOS logic gates,<br>a) Full swing with shunting device,<br>b) Full swing complementary MOS/Bipolar Logic circuit. | [L1][CO1] | **[6M]** |
| 3. | | What are all the performance evaluation and comparison of BiCMOS logic gates? | [L1][CO2] | **[12M]** |
| 4. | | With suitable diagram, explain the merged BiCMOS digital circuits. | [L3][CO1] | **[12M]** |
| 5. | a) | Explain in detail about performance evaluation of merged BiCMOS digital circuits. | [L1][CO1] | **[6M]** |
| | b) | Discuss the experimental result of merged BiCMOS digital circuits. | [L1][CO3] | **[6M]** |
| 6. | | Explain the following parameters in ESD-free BiCMOS Digital circuits,<br>a) Circuit operation.<br>b) Comparative evaluation. | [L2][CO1] | **[12 M]** |
| 7. | | Explain the following Bootstrapped-type BiCMOS digital circuits,<br>a)1.5V logic gate,<br>b)Full swing Inverter. | [L2][CO3] | **[12M]** |
| 8. | | Describe the operation of High beta BiCMOS digital circuits and analyze its performance. | [L1][CO1] | **[12M]** |
| 9. | a) | Explain BiNMOS version of Bootstrapped circuit with neat sketch | [L2][CO1] | **[6M]** |
| | b) | What are the design considerations of 1.5V Bootstrapped Full swing BiCMOS/BiNMOS inverter? | [L1][CO3] | **[6M]** |
| 10. | a) | Explain the working of twin capacitor BiNMOS logic gate and evaluate its performance. | [L2][CO3] | **[6M]** |
| | b) | Explain Feedback-Type BiCMOS digital circuits. | [L1][CO1] | **[6M]** |

Course code: **20EC4210** **R20**

## UNIT –IV
## LOW POWER LATCHES AND FLIP FLOPS

| | | | | |
|---|---|---|---|---|
| 1. | a) | Explain about the functionality and the synchronous theme in the evolution of latches and flip. | [L2][CO1] | **[6M]** |
| | b) | Explain about the optimization and the performance theme in the evolution of latches and flip. | [L1][CO3] | **[6M]** |
| 2. | a) | Explain about the pipelining theme in the evolution of Latches and Flip-flop. | [L2][CO3] | **[6M]** |
| | b) | Explain about the high performance and low power theme in the evolution of latches and Flip-flop. | [L2][CO1] | **[6M]** |
| 3. | a) | Discuss about the maximum operation clock frequency and setup and hold time consideration in performance measures for latches and Flip-flop. | [L3][CO2] | **[6M]** |
| | b) | Discuss about the sensitivity to clock skew and input and clock skew rate of performance measures for latches and Flip-flop. | [L1][CO2] | **[6M]** |
| 4. | | Interpret the measurement of power dissipation measure in latches and Flip-flops. | [L2][CO1] | **[12M]** |
| 5. | | Explain in detail about Dynamic flip-flops in single edge-triggered Flip-flops. | [L1][CO3] | **[12M]** |
| 6. | | Explain in detail about Double edge-triggered Flip-flops. | [L2][CO3] | **[12M]** |
| 7 | a) | Describe static and semi static Flip-flops with neat diagrams. | [L1][CO3] | **[6M]** |
| | b) | What is meant by Synchronous theme of Flip-flops? | [L1][CO2] | **[6M]** |
| 8 | | Explain High-performance and Low power theme of CMOS. | [L1][CO1] | **[12M]** |
| 9 | | Explain the following terms:<br>a)MOCF.<br>b)Clock skew. | [L2][CO1] | **[12M]** |
| 10. | | Explain the following performance measures of a latch/Flip-flop<br>a) Full swing Considerations.<br>b) MOCF. | [L1][CO3] | **[12M]** |

## UNIT V
## SPECIAL TECHNIQUES

| | | | | |
|---|---|---|---|---|
| 1. | a) | Explain in detail about clock gating in clock networks. | [L1][CO1] | **[6M]** |
| | b) | How the swing clock is used to reduce the power in clock networks? | [L1][CO3] | **[6M]** |
| 2. | a) | Describe the Oscillator Circuit for Clock Generation. | [L1][CO2] | **[6M]** |
| | b) | Explain about Frequency Division and Multiplication. | [L2][CO1] | **[6M]** |
| 3. | a) | Discuss Tristate Keeper Circuit in CMOS Floating Node. | [L3][CO2] | **[6M]** |
| | b) | Explain in detail about Blocking Gate in CMOS Floating Node. | [L1][CO2] | **[6M]** |
| 4. | a) | Interpret Low Swing Bus with suitable diagram. | [L2][CO1] | **[6M]** |

| | | | | |
|---|---|---|---|---|
| | b) | Explain the Recycling Bus in low power bus. | [L3][CO2] | **[6M]** |
| 5. | | Discuss how delay can be balanced in low power bus. | [L1][CO2] | **[12M]** |
| 6. | a) | How SRAM Cell is used for low power techniques. | [L1][CO1] | **[6M]** |
| | b) | Explain about Pulsed Word line and Reduced Bit line Swing. | [L1][CO2] | **[6M]** |
| 7. | | Briefly describe CMOS Floating node. | [L2][CO2] | **[12M]** |
| 8. | | Explain various delay balancing techniques with a neat sketch. | [L3][CO2] | **[12M]** |
| 9. | a) | Explain different low power techniques for SRAM. | [L1][CO1] | **[6M]** |
| | b ) | What is SRAM? Draw the circuit of SRAM. | [L2][CO1] | **[6M]** |
| 10. | a) | What is meant by Clock Distribution Network? | [L3][CO2] | **[6M]** |
| | b) | What is Resonant clocking? | [L1][CO2] | **[6M]** |

***Prepared by: Raghul G***